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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VERDERAMO III, RALPH	
ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/584,778	XIONG, GUOPING	
	Examiner	Art Unit	
	RALPH A. VERDERAMO III	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 3 is objected to because of the following informalities: Claim 3 states "judging whether the processing of the first programming or erasing **instructions** is finished". Claim 1 was amended to only recite "programming or erasing **instruction**". Claim 3 should be amended similarly and will be interpreted in view of claim 1 for the purpose of further examination. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ng et al. US Patent Application Publication No. 2005/0010717 (herein after referred to as Ng) in view of Estakhri et al. US Patent No. 6081878 (herein after referred to as Estakhri).

Regarding claim 1, Ng describes A data write-in method for a flash memory, wherein the system comprises at least two flash chips (two flash memory cells (page 3, paragraph [0046])) and a controller (controller (page 4, paragraph [0068]), and the method comprises: partitioning physical blocks in the flash chips to odd logical block addresses and even logical block addresses, respectively; the controller receiving a data write-in instruction and analyzing a beginning logical address for writing from the received data write-in instruction; the controller obtaining the logical block address needed to be written according to the analyzed beginning logical address; the controller determining a parity of the logical block address, and selecting one flash chip from the flash chips according to the determined parity of the logical block address (In step (100), the host issues reading/writing signal…Step (220), is the writing step...In step (220), whether the target page for writing is odd or even is determined (page 3, paragraphs [0047] - [0050])); the controller directing a first programming or erasing instruction to the physical blocks corresponding to the obtained logical block address in the selected flash chip (If the page is odd, then the process proceeds to step (340). If the page is even, then the process proceeds to step (330) (page 3, paragraph [0050]). In step (330), writing data into the first flash memory cell 330 is commenced, then the process proceeds to step (420) (page 3, paragraph [0053])); the controller detecting whether the other flash chip needs to be programmed or erased while the first programming or erasing instruction is being processed (In step (420), whether to continue writing data is determined. If

yes, the process returns to step (220), if not the process skips to (500) (page 4, paragraph [0056]). In step (220), whether the target page for writing is odd or even is determined (page 3, paragraph [0050])); if programming or erasing is needed in the other flash chip, the method further comprises: the controller directing a second programming or erasing, instruction to the other flash chip of at least two flash chips (If the page is odd, then the process proceeds to step (340). If the page is even, then the process proceeds to step (330) (page 3, paragraph [0050]). In step (340), writing data into the second flash memory cell 340 is commenced, then the process proceeds to step (420) (page 4, paragraph [0054]). See also, Fig. 3). Ng does not specifically describe that a flash memory comprises the at least two flash chips and the controller.

Estakhri describes a method for increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash memory devices. Furthermore Fig. 6 shows a flash memory comprising a controller 510 coupled to two flash memory chips 670 and 672 (column 6, lines 23 – 52). Estakhri shows that this is a common set up for a flash memory (which is further shown since it is similar to the set up presented as prior art in Fig. 1) and that the flash memory may write in an interleaved manner that improves speed (Fig. 13 shows even sectors in one chip and odd sectors in the other).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a flash memory comprising at least two chips and a controller as described by Estakhri in the invention of Ng because Estakhri

shows that it is a conventional flash memory (Fig. 1 similar to Fig. 6) and that interleaving may be accomplished in such a setting (Fig. 13).

Regarding claim 3, Ng describes the data write-in method for a flash memory according to claim 1 (see above), wherein if the other flash chip does not need to be programmed or erased, the method further comprises: judging whether the processing of the first programming or erasing instruction is finished (In step (420), whether to continue writing data is determined. If yes, the process returns to step (220), if not, the process skips to (500) (Ng, page 4, paragraph [0056])).

Regarding claim 6, Ng describes the data write-in method for a flash memory according to claim 1 (see above), wherein the analyzing further comprises: obtaining the number of sectors needed to be written from the data writing operation instruction (sector counter (Ng, page 6, paragraph [0109])).

Regarding claim 7, Ng describes the data write-in method for a flash memory according to claim 6 (see above), the analyzing further comprises: judging whether the data write-in instruction has been finished by subtracting a number of written sectors from a number of need-to-be-written-sectors (Step 7, use the Sector_Counter to reduce two then judging whether it is 0... (Ng, page 6, paragraph [0115])).

Response to Arguments

5. Applicant's arguments with respect to claims 1, 3, 6 and 7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Sukegawa US Patent No. 5572466 – describes how multiple chips may be written to simultaneously (column 9, line 44 - column 10, line 13);

Nakanishi et al. US Patent No. 7633817 – Fig. 8 shows how odd L.S. No. end up in F10 and F11 (same area shown in Fig. 1) and even L.S. No. end up in F00 and F01 (again same area shown in Fig. 1);

Gorobets US Patent No. 7215580 – Fig. 7 shows 2 flash chips, one with odd sectors and one with even sectors;

Norris et al. US Patent No. 5453957 – describes how conventional interleaved memory provides an "even" memory bank and an "odd" memory bank (column 2, lines 28 - 44);

Han et al. US Patent Application Publication No. 2004/0111583 – Paragraph [0079] describes how even numbered sectors are included in the first memory bank and odd sectors are included in the second memory bank. Fig. 15 shows the idea of starting a write to one bank then seeing if more data needs to be written to the other bank;

Hasbun US Patent No. 5671388 – describes that blocks are arranged in flash EEPROM chip pairs, such that one block integrates the use to two flash EEPROM integrated circuit chips in an odd and even chip pair arrangement (column 5, lines 10 – 20);

Gan et al. US Patent Application Publication No. 2005/0005058 –

describes a similar invention to previously cited Ng.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RALPH A. VERDERAMO III whose telephone number is (571)270-1174. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ralph A Verderamo III/
Examiner, Art Unit 2186

/Shane M Thomas/
Primary Examiner, Art Unit 2186

rv
February 20, 2011